REMARKS

In response to the Office Action dated February 11, 2009, Applicant requests consideration of the foregoing amendments and the following remarks. Claims 1, 7, 9, 10, 13, 17, 18, and 22 are amended, and claims 5 and 16 are cancelled. Claims 1-4, 6-15, and 17-22 are currently pending in the application. Amendments to the Specification are made to correct minor errors noted during review, and to include patent application numbers of related applications. No new matter has been added by virtue of the amendments.

I. Objection to the Drawings

The Drawings are objected to because "Iteration N" is misspelled as "It ration N" in FIG. 4. The amendments the Drawings include an amendment to Figure 4, which Applicant believes to overcome the objection. In addition to amending Figure 4 in order to overcome the objection, Applicant also submits herewith an additional amendment to Figure 4, to correct "PROCESSING ITERATION N+1" in state 44 to "PROCESSING ITERATION N+2." Applicant respectfully requests that the amendment be entered, and that the objection to the drawings be withdrawn.

II. Claim Rejections - 35 U.S.C. § 102

Claims 13-15 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Publication No. 2002/0176489 to Sririam et al. (herein "Sririam"). Applicant has amended claim 13, from which the remaining rejected claims depend, and respectfully traverses this rejection.

Sririam discloses a vector correlator based Rake receiver that employs a circular buffer (para. [0007]). Two of the three buffers are available for processing by a correlator datapath while the remaining buffer is being written into by incoming chips (para. 0009]). The triple data buffer implements a sliding buffer of 16-chips in which the buffer slides by an interval of 16-chips in a circular fashion in each iteration (FIG. 1 and para. 0040]). At each correlator co-processor (CCP) iteration32-chips from the 48-chip triple data input buffer 100 are available for processing by the CCP datapath. At the next iteration, a new set of 16-chips, along with an older set of 16-chips, becomes available to the datapath (FIG. 1 and para. [0040]).

Applicant's claims 13-15 include at least the following features, which differentiate claims 13-15 from that which is disclosed by Sririam:

". . . processing, by a processor during a first symbol group duration, the symbols in a first group of sample buffers and receiving digital samples from the receiver at a second group of sample buffers during the processing;

disabling the processor upon completion of processing the symbols in the first group of sample buffers through a remainder of the symbol group duration; and

enabling the processor to process the symbols in the second group of sample buffers during a second symbol group duration"

Sririam does not disclose each and every feature of claims 13-15. More particularly, Sririam does not disclose disabling a processor upon completion of processing symbols in a symbol group for a remainder of a symbol group duration.

Based on the amendments and the above remarks, Applicant believes that the rejection of claims 13-15 under 35 U.S.C. 102(e) has been overcome. Accordingly, Applicant respectfully requests that this rejection be reconsidered and withdrawn, and that claims 13-15 be allowed.

III. Claim Rejections - 35 U.S.C. § 103

Claims 1-4, 6-7, 9-12, 17, and 22:

Claims 1-4, 6-7, 9-12, 17, and 22 are rejected under 35 U.S.C. §103(a) as being unpatentable over Sririam in view of U.S. Patent No. 6,351,714 to Birchmeier (herein "Birchmeier"). Applicant has amended claims 1, 9, 10, 17, and 22, from which the remaining rejected claims depend, and respectfully traverses this rejection.

The Sririam reference was previously discussed. Birchmeier discloses a data collector 20 (FIG. 1) that includes a field programmable gate array (FPGA) 74 and a digital signal processor (DSP) 82 (FIG. 1 and col. 4, lines 48-61). The FPGA 74 provides an interrupt to the DSP 82, and with each interrupt, the DSP 82 processes samples of a vibration signal and samples of a reference signal. The DSP 82 must complete its processing of the vibration and reference signals prior to receiving the next interrupt from the FPGA 74.

Applicant's claims 1-4 and 6-7, include at least the following features, which differentiate claims 1-4 and 6-7 from that which is disclosed by Sririam and Birchmeier:

". . . buffering first digital samples corresponding to a first group of symbols into a first buffer and a second buffer, wherein buffered first digital samples corresponding to earlier paths of the first group of symbols are stored in the first buffer, and buffered first digital samples corresponding to later paths of the first group of symbols are stored in the second buffer;

processing, by the processor, the first digital samples in the first buffer and the second buffer for all known paths of the first group of symbols during a first symbol group duration;

disabling the processor upon completion of processing the first digital samples through a remainder of the first symbol group duration . . ."

Independent claims 9, 10 (from which claims 11 and 12 depend), 17, and 22 include similarly distinguishing features, which are not repeated here for the purpose of brevity.

Neither Sririam, Birchmeier nor their combination discloses each and every feature of claims 1-4, 6-7, 9-12, 17, and 22. More particularly, nowhere do Sririam or Birchmeier disclose disabling a processor upon completion of processing symbols in a symbol group for a remainder of a symbol group duration.

Based on the amendments and the above remarks, Applicant believes that the rejection of claims 1-4, 6-7, 9-12, 17, and 22 under 35 U.S.C. 103(a) has been overcome. Accordingly, Applicant respectfully requests that this rejection be reconsidered and withdrawn, and that claims 1-4, 6-7, 9-12, 17, and 22 be allowed.

Claim 5:

Claim 5 is rejected under 35 U.S.C. §103(a) as being unpatentable over Sririam and Birchmeier in view of U.S. Patent No. 6,650,140 to Lee et al. (herein "Lee"). Applicant has cancelled claim 5, and therefore this rejection is now moot.

Claim 8:

Claim 8 is rejected under 35 U.S.C. §103(a) as being unpatentable over Sririam and Birchmeier in view of U.S. Patent No. 6,714,527 to Kim et al. (herein "Kim"). Applicant has amended claim 1, from which claim 8 depends, and respectfully traverses this rejection.

The Sririam and Birchmeier references were previously discussed. Kim discloses a multiuser detector 17 for detecting, after reception, a plurality of users transmitting over a common CDMA channel, where a corresponding plurality of communication signals have different spreading codes (Abstract, lines 1-2; col. 1, lines 15-21; FIG. 7; and col. 8, lines 48-50). When the spreading codes are orthogonal to one another, the received signal can be correlated with a particular user signal related to the particular spreading code such that only the desired user signal related to the particular spreading code is enhanced, while the other signals for all other users are not enhanced (col. 1, lines 60-65).

As discussed above in conjunction with the response to the rejection of claim 1, neither Sririam, Birchmeier nor their combination disclose each and every feature of claim 1. Accordingly, neither Sririam, Birchmeier nor their combination disclose each and every feature of claim 8. Kim does not make up for the deficiencies in Sririam and Birchmeier. Accordingly, neither Sririam, Birchmeier, Kim nor their combination disclose each and every feature of claim 8.

Based on the amendments and the above remarks, Applicant believes that the rejection of claim 8 under 35 U.S.C. 103(a) has been overcome. Accordingly, Applicant respectfully requests that this rejection be reconsidered and withdrawn, and that claim 8 be allowed.

Claim 16:

Claim 16 is rejected under 35 U.S.C. §103(a) as being unpatentable over Sririam in view of U.S. Patent Publication No. 2002/0176489 to Roohparvar (herein "Roohparvar"). Applicant has cancelled claim 16, and therefore this rejection is now moot.

Claims 18-21:

Claims 18-21 are rejected under 35 U.S.C. §103(a) as being unpatentable over Sririam in view of Birchmeier, and further in view of U.S. Patent Publication No. 2001/0038633 to Robertson et al. (herein "Robertson"). Applicant has amended claim 18, from which the remaining rejected claims depend, and respectfully traverses this rejection.

The Sririam and Birchmeier references were previously discussed. Robertson discloses a network switch system 10 in which a clock frequency compensation FIFO 34 having a circular buffer 44 is implemented (FIG. 6, and para. [0052]). The circular buffer 44 has five entries, where each entry is associated with an instance of receive/transmit valid logic (FIG. 6, para. [0051]).

Applicant's claims 18-21 include at least the following features, which differentiate claims 18-21 from that which is disclosed by Sririam, Birchmeier, and Robertson:

". . . processing, by the processor during a first symbol group duration, from all known paths of a first group of symbols, wherein buffered digital samples corresponding to the first group of symbols start in a first buffer and end in a third buffer, and receiving samples at a fourth buffer and a fifth buffer while the first group of symbols is being processed;

disabling the processor upon completion of processing the first group of symbols during a remainder of the first symbol group duration . . ."

Neither Sririam, Birchmeier, Robertson nor their combination discloses each and every feature of claims 18-21. More particularly, nowhere do Sririam, Birchmeier or Robertson disclose disabling a processor upon completion of processing a group of symbols for a remainder of a symbol group duration.

Based on the amendments and the above remarks, Applicant believes that the rejection of claims 18-21 under 35 U.S.C. 103(a) has been overcome. Accordingly, Applicant respectfully requests that this rejection be reconsidered and withdrawn, and that claims 18-21 be allowed.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending are in condition for allowance. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (480) 385-5060. If necessary, the Commissioner is hereby authorized to charge payment or credit any overpayment to Deposit Account No. 50-2091 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly extension of time fees.

Respectfully submitted,

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